ERRATA SHEET

Date: **2007 March 22**
Document Release: **Version 1.1**
Device Affected: **LPC2368**

This errata sheet describes both the functional deviations and any deviations from the electrical specifications known at the release date of this document.

Each deviation is assigned a number and its history is tracked in a table at the end of the document.

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NXP
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Document revision history

Rev	Date	Description
1.0	November 14, 2006	First version
1.1	March 22, 2007	1. Corrected the value of M in PLL.1 2. Updated ESD.1 3. Added core.1

Identification

The typical LPC2368 devices have the following top-side marking:

LPC2368xxx

xxxxxxx

xxYYWW R

The last letter in the third line (field ‘R’) will identify the device revision. This Errata Sheet covers the following revisions of the LPC2368:

Revision Identifier (R)	Comment
‘-’	Initial device revision

Field ‘YY’ states the year the device was manufactured. Field ‘WW’ states the week the device was manufactured during that year.

Errata Overview - Functional Problems

Functional Problem	Short Description	Device Revision
ADC.1	ADDRx read conflicts with hardware setting of DONE bit	-
Ethernet.1	Setting up the Ethernet interface in RMII mode	-
Ethernet.2	Ethernet SRAM disabled	-
I^2S.1	I^2S DMA can stall	-
PLL.1	PLL output is limited to 290MHz	-
SRAM.1	16kB SRAM can not be used for code execution	-
USB.1	USB_NEED_CLK is always asserted	-
USB.2	U1CONNECT is not functional	-
USB.3	V_{BUS} status input is not functional	-
WDT.1	Accessing non-Watchdog APB registers in the middle of the feed sequence causes a reset	-
Core.1	Incorrect update of the Abort Link register in Thumb state	-

Errata Overview - AC/DC Deviations

AC/DC Deviation	Short Description	Device Revision
ESD.1	2kV ESD requirements are not met on the RTCX1 pin	-

Errata Notes

Note	Short Description
NA	NA

Functional Deviations of LPC2368

ADC.1: ADDRx read conflicts with hardware setting of the DONE bit

Introduction: The LPC2368 has a 10-bit ADC, which can be used to measure analog signals and convert the signals into a 10-bit digital result. There are eight A/D channels and each channel has its own individual A/D Data Register (ADDR0-ADDR7). The A/D Data Register holds the result when an A/D conversion is complete, and also includes the flags that indicate when a conversion has been completed (DONE bit) and when a conversion overrunhas occurred. The DONE bit is cleared when the respective A/D Data Register is read.

Problem: If a software read of ADDRx conflicts with the hardware setting of the DONE bit in the same regis ter (once a conversion is completed) then the DONE bit gets cleared automatically, thereby clearing the indication that a conversion was completed.

Workarounds: For software controlled mode or burst mode with only one channel selected, the DONE bit in the A/D Global Data Register (located at 0xE003 4004) can be used instead of the individual ADDRx result register with no impact on performance.

For burst mode with multiple channels selected, the DONE bit together with the CHN field in the A/D Global Data Register can be used with some impact on throughput.

Ethernet.1: Setting up the Ethernet interface in RMII mode

Introduction: The LPC2368 has an Ethernet interface, which can be interfaced with an off-chip PHY using the RMII interface only. The MII interface is not supported on this device.

Problem: The default configuration of the device does not enable the RMII interface.

Workaround: To use the Ethernet interface in RMII mode write a 1 to bit 12 in PINSEL2 register (located at 0xE002 C008).

Ethernet.2: Ethernet SRAM disabled

Introduction: The LPC2368 has an Ethernet interface, which has a dedicated 16kB SRAM.

Problem: When the Ethernet block is disabled (in the PCONP register located at 0xE01F C0C4), the Ethernet SRAM is also disabled.

Workaround: Enable the Ethernet block by setting the PCENET bit (bit no 30) in the PCONP register. The Ethernet SRAM is now enabled.

I^2S.1: I^2S DMA interface is non-operational

Introduction: The LPC2368 has an I^2S interface, which can be used for audio devices. The I^2S interface was initially designed to operate with the general purpose DMA controller.

Problem: The DMA controller cannot access the I^2S interface.

Workaround: No known workaround.

PLL.1: PLL output (F_{CCO}) is limited to 290MHz

Introduction: The PLL input, in the range of 32 KHz to 50 MHz, may initially be divided down by a value"N", which may be in the range of 1 to 256. Following the PLL input divider is the PLL multiplier. This can

multiply the input divider output through the use of a Current Controlled Oscillator (CCO) by a value "M", in the range of 1 through 32768. The resulting frequency, F_{CCO} must be in the range of 275 MHz to 550 MHz.This frequency can be divided down (using the Clock Divider registers) to get the desired clock frequencies for the core and peripherals.

Problem: The maximum output of the CCO within the PLL block is limited to 290MHz.

Workaround: Care should be taken while programming the PLL so that F_{cco} resides in the desired range. The suggested setting is to use a 12MHz external crystal. Use a PLLdivider (N) of 1 and PLL multiplier (M) of 12. Putting the values in the equation:

$F_{CCO} = (2 \times M \times F_{IN}) / N$

Fcco= 288MHz

The CPU Clock Configuration register (located at 0xE01F C104) can then be used to divide this frequency by 4 to produce the maximum CPU speed of 72MHz.

SRAM.1: 16kB SRAM cannot be used for code execution

Introduction: The LPC2368 has 16kB of SRAM on the AHB2 bus, which would generally be used by the Ethernet block.

Problem: The 16kB of SRAM can only be used as data RAM. Code can not be executed from this memory.

Workaround: No known workaround.

USB.1: USB_NEED_CLK is always asserted

Introduction: The USB_NEED_CLK signal is used to facilitate going into and waking up from chip Power Down mode. USB_NEED_CLK is asserted if any of the bits of the USBClkSt register are asserted.

Problem: The USB_NEED_CLK bit of the USBIntSt register (located at 0xE01F C1C0) is always asserted, preventing the chip from entering Power Down mode when the USBWAKE bit is set in the INTWAKE register (located at 0xE01F C144).

Workaround: After setting the PCUSB bit in PCONP (located at 0xE01F C0C4), write 0x1 to address 0xFFE0C008. The USB_NEED_CLK signal will now function correctly. Writing to address 0xFFE0C008 only needs to be done once after each chip reset.

USB.2: U1CONNECT signal is not functional

Introduction: U1CONNECT Signal (alternate function of P2.9) is part of the SoftConnect USB feature, which is used to switch an external 1.5 KOhm resistor under the software control.

Problem: The USB U1CONNECT alternate function does not work as expected.

Workaround: Configure P2.9 as a GPIO pin, and use it to enable the pull-up resistor on the U1D+ pin.

USB.3: V_{BUS} status input is not functional

Introduction: The V_{BUS} signal indicates the presence of USB bus power.

Problem: The V_{BUS} status input is not functional.

Workaround: Configure P1.30 as a GPIO pin, and poll it to determine when V_{BUS} goes to 0, signalling a disconnect event.

WDT.1: Accessing non-Watchdog APB registers in the middle of the feed sequence causes a reset.

Introduction: The Watchdog timer can reset the microcontroller within a reasonable amount of time if it enters an erroneous state.

Problem: After writing 0xAA to WDFEED, any APB register access other than writing 0x55 to WDFEED may cause an immediate reset.

Workaround: Avoid APB accesses in the middle of the feed sequence. This implies that interrupts and the GPDMA should be disabled while feeding the Watchdog.

Core.1 Incorrect update of the Abort Link register in Thumb state

Introduction: If the processor is in Thumb state and executing the code sequence STR, STMIA or PUSH followed by a PC relative load, and the STR, STMIA or PUSH is aborted, the PC is saved to the abort link register.

Problem: In this situation the PC is saved to the abort link register in word resolution, instead of half-word resolution.

Conditions:

The processor must be in Thumb state, and the following sequence must occur:

<any instruction>

<STR, STMIA, PUSH> <---- data abort on this instruction

LDR rn, [pc,#offset]

In this case the PC is saved to the link register R14_abt in only word resolution, not half-word resolution. The effect is that the link register holds an address that could be #2 less than it should be, so any abort handler could return to one instruction earlier than intended.

Work around: In a system that does not use Thumb state, there will be no problem.

In a system that uses Thumb state but does not use data aborts, or does not try to use data aborts in a recoverable manner, there will be no problem.

Otherwise the workaround is to ensure that a STR, STMIA or PUSH cannot precede a PC-relative load. One method for this is to add a NOP before any PC-relative load instruction. However this is would have to be done manually.

Electrical and Timing Specification Deviations of LPC2368

ESD.1: The LPC2368 does not meet the 2kV ESD requirements on the RTCX1 pin

Introduction: The LPC2368 is rated for 2kV ESD.The RTCX1 pin is the input pin for the RTC oscillator circuit.

Problem: The LPC2368 does not meet the required 2kV ESD specified.

Workarounds: Observe proper ESD handling precautions for the RTCX1 pin.

Errata Notes

No known Errata Notes