UH7843Q/S/AQ/AS

TOUCH SCREEN CONTROLLER

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Version: V 2.3
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■ This data sheet is subject to change without notice.

FEATURES

- Serial interface
- 4-wire touch screen interface
- Embedded touch screen drivers
- 2.2V to 3.6V/5V supply voltage
- 12-bit analog to digital converter
- Programmable 8- or 12-bit resolution
- Up to 125KHz conversion rate
- 2 auxiliary analog inputs
- Full power-down control
- 16-pin SSOP or QFN package
- RoHS Compliant and 100% Lead (Pb) Free

APPLICATIONS

- Touch screens
- Personal digital assistants (PDA)
- Smart phones
- Point-to-sales terminals
- High speed data acquisition
- Portable instruments
- Low power instruments

Ordering Information

PART	PACKAGE	RoHS
UH7843S	SSOP-16	Yes
UH7843Q	QFN-16	Yes
UH7843AS	SSOP-16	Yes
UH7843AQ	QFN-16	Yes

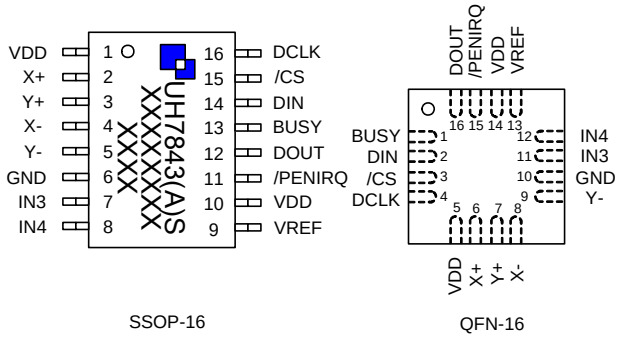
DESCRIPTION

UH7843Q/S/AQ/AS touch screen controller IC is a 12-bit SAR analog-to-digital (ADC) converter with SPI serial interface and low on-resistance drivers for 4-wire resistive touch screens.

UH7843Q/S/AQ/AS is a highly integrated controller for portable applications with 4-wire resistive touch screen such as PDA, UMPC, portable instruments, cellular phone and so on. UH7843Q/S/AQ/AS contains all the analog and digital circuitry necessary to complete a pen request.

UH7843Q/S/AQ/AS consumes only 648uW at a 125KHz sample rate and a 2.7V power supply and consumes only 2.7uW at shutdown mode. UH7843Q/S/AQ/AS is guaranteed to operate with power supply 2.2V to 3.6V/5V. UH7843Q/S/AQ/AS is provided in a small 16-pin SSOP or QFN package.

Pin Configuration



Absolute Maximum Rating

VDD to GND ……..–0.3V to +3.6V/6V
Analog Input to GND …….. -0.3V to VDD+0.3V
Digital Input to GND …….. -0.3V to VDD+0.3V
Operating Temperature Range ……..….. -40˚C to +85˚C
Maximum Junction Temperature …..……...…… +150˚C
Storage Temperature Range ……..... -60˚C to 150˚C
Lead Temperature (Soldering 10s) ……..…..…… +300˚C
ESD Susceptibility
HBM (Human Body Mode)……..±5500V
MM (Machine Mode)……..….±200V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electro-Static Discharge Sensitivity

This integrated circuit can be damaged by ESD. It is recommended that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure.

Pin Description

QFN PIN	SSOP PIN	Name	Description
5	1	**VDD**	Power supply, 2.2V to 3.6V/5.0V
6	2	**X+**	X+ input or ADC input channel 1
7	3	**Y+**	Y+ input or ADC input channel 2
8	4	**X-**	X- input.
9	5	**Y-**	Y- input.
10	6	**GND**	Ground.
11	7	**IN3**	Auxiliary input1 or ADC input channel 3
12	8	**IN4**	Auxiliary input 2 or ADC input channel 4
13	9	**VREF**	Reference voltage input
14	10	**VDD**	Power supply, 2.2V to 3.6V/5.0V
15	11	**/PENIRQ**	Pen interrupt; Requires 10KΩ to 100KΩ external pull-up resistor.
16	12	**DOUT**	Serial data output; This output pin is high impedance when **/CS** is high.
1	13	**BUSY**	Busy output; This output pin is high impedance when **/CS** is high.
2	14	**DIN**	Serial data input
3	15	**/CS**	Chip select input; This input is active low.
4	16	**DCLK**	External clock input

Block Diagram

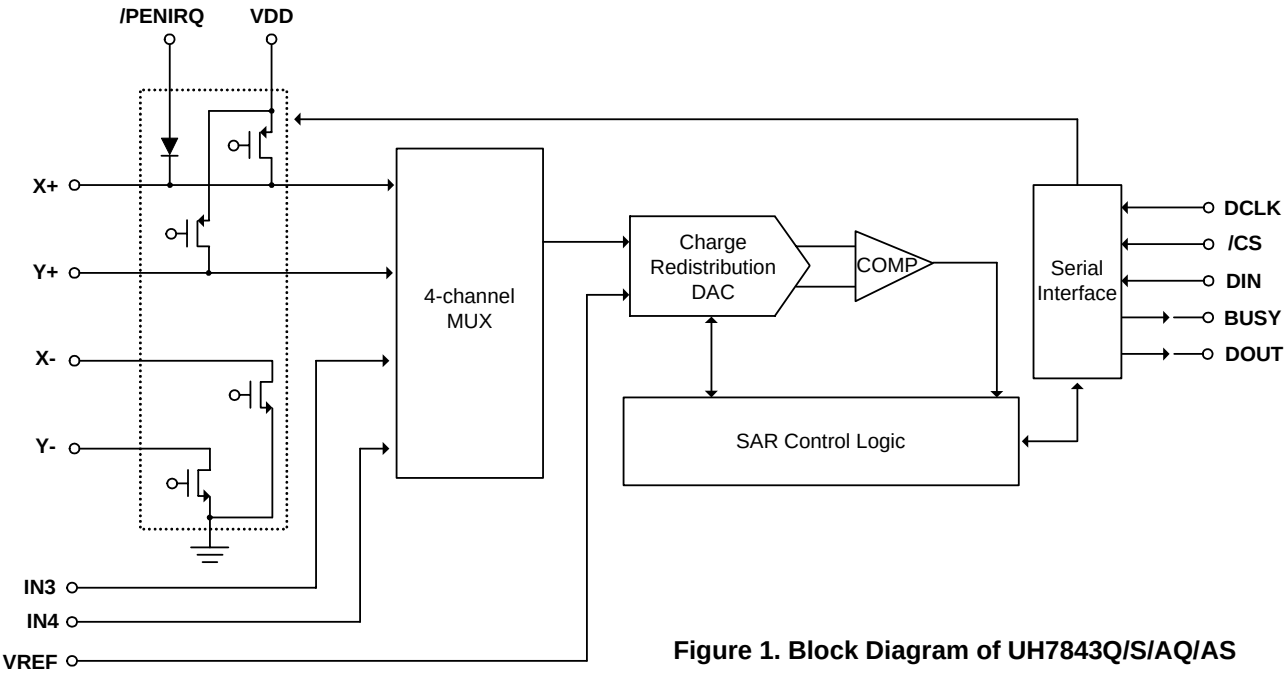


Figure 1. Block Diagram of UH7843Q/S/AQ/AS

Electrical Specifications

(T_A=-40°C to 85°C, VDD=+2.7V, V_{REF}=+2.7V, f_{sample}=125KHz, f_{CLK}=24*f_{sample}, 12-bit mode, Digital inputs=GND or VDD. Typical values are at T_A=+25°C, unless otherwise noted.)

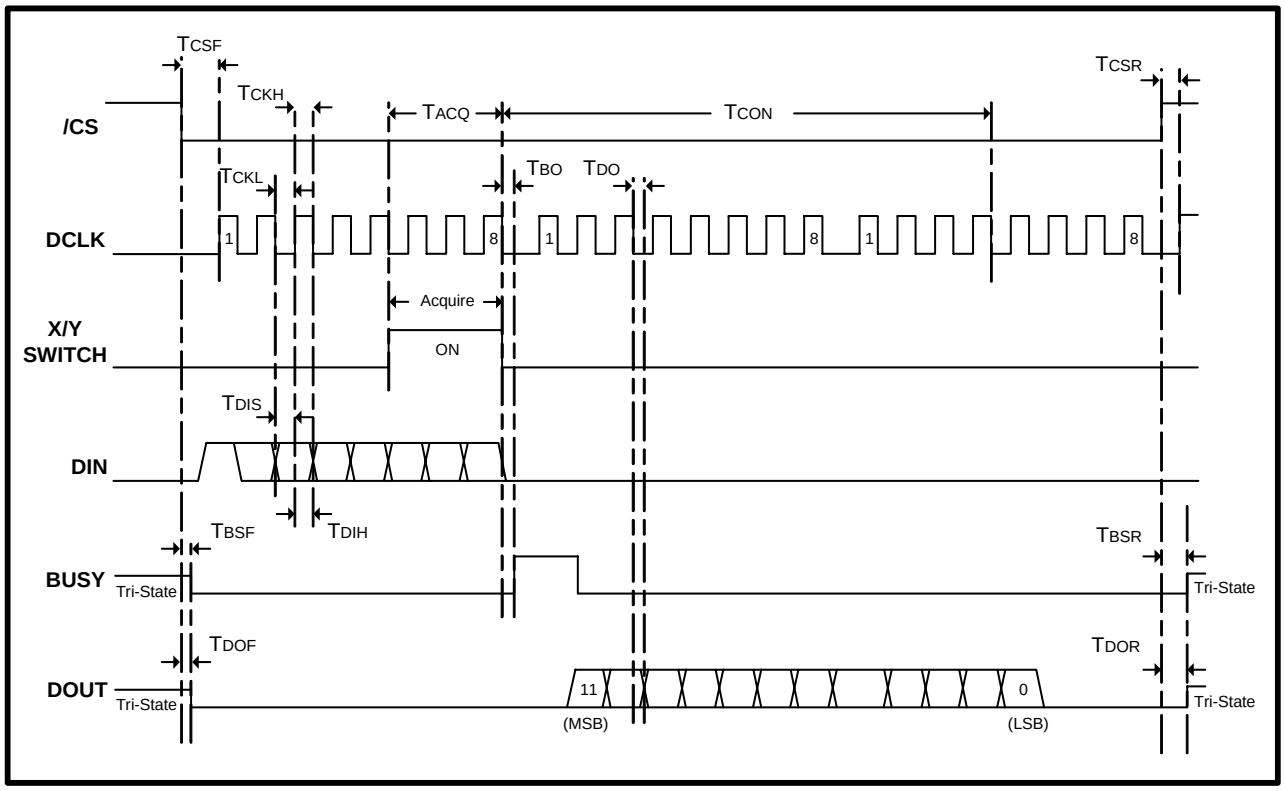
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Requirements					
VDD	Specified Performance	2.7		3.6	V
UH7843Q/S	Operating Range	2.2		3.6	V
UH7843AQ/AS	Operating Range	2.2		5	V
Nominal Supply Current			240		µA
	Shut Down Mode			1	µA
Power Dissipation			648		µW
	Shut Down Mode			2.7	µW
System Performance					
Resolution			12		Bit
INL			+/-2		LSB
DNL			+/-1		LSB
Gain Error			+/-4		LSB
Offset Error			+/-6		LSB
Digital Input/Output					
Logic Family	CMOS				
V_{OH}		VDD * 0.8			V
V_{OL}				0.4	V
V_{IH}		VDD * 0.7		VDD + 0.3	V
V_{IL}		-0.3		0.8	V
/PENIRQ	100KΩ Pull-Up				
V_{OL}			0.6		V
Analog Input					
Input Span		0		V_{REF}	V
Input Range		-0.2		VDD+0.2	V
Capacitance			25		pF
Reference Input					
Range		1		VDD	V
Input Current	Specified Performance		15		µA
X / Y Switches					
X+, Y+	Switch On-Resistance		5		Ω
X-, Y-	Switch On-Resistance		5		Ω
Temperature Range					
Operating Temperature Range	Specified Performance	-40		+85	°C

Timing Specifications

(T_A=-40°C to 85°C, VDD≧+2.7V, C_{LOAD}=50pF. Typical values are at T_A=+25°C, unless otherwise noted.)

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{ACQ}	ADC acquisition time	500			ns
T_{CON}	ADC conversion time	6.5			μs
T_{CSF}	/CS falling to first DCLK rising	100			ns
T_{CSR}	/CS rising to DCLK ignored	0			ns
T_{DOF}	/CS falling to DOUT enable			200	ns
T_{DOR}	/CS rising to DOUT disable			200	ns
T_{BSF}	/CS falling to BUSY enable			200	ns
T_{BSR}	/CS rising to BUSY disable			200	ns
T_{CKH}	DCLK high period	200			ns
T_{CKL}	DCLK low period	200			ns
T_{DIS}	DIN valid before DCLK rising	100			ns
T_{DIH}	DIN hold time after DCLK going high	15			ns
T_{DO}	DCLK falling to DOUT valid			200	ns
T_{BO}	DCLK falling to BUSY rising			200	ns

Timing Diagram



FUNCTIONAL DESCRIPTION

Overview

UH7843Q/S/AQ/AS is a 12-bit switched capacitor analog-to-digital converter. The converter is fabricated with a 0.6um CMOS process and packaged in the small 16-pin SSOP or QFN package.

The typical operation of UH7843Q/S/AQ/AS is shown in Figure 8. UH7843Q/S/AQ/AS operates in a single power supply ranging from +2.2V to 3.6V/5V. It requires an external reference voltage and an external clock. The reference voltage directly sets the input range of the converter.

UH7843Q/S/AQ/AS contains four channel inputs, a serial interface and low on-resistance switches for touch screen (see Block Diagram). The input to the converter is selected via the four-channel multiplexer as shown in Figure 5.

Serial Interface

The typical operation of UH7843Q/S/AQ/AS' serial interface (/CS, DCLK, DIN and DOUT) is shown in Figure 2. UH7843Q/S/AQ/AS communicates with microprocessors or digital signal processors via a synchronous serial interface. One complete conversion can be accomplished with three serial communications for a total 24 clock cycles of DCLK.

Operation of 24-clocks

The operation is initiated by a falling signal on Chip Select (/CS) input. After /CS falls, UH7843Q/S/AQ/AS looks for a start bit on DIN input. The first eight clock cycles are used to provide the control byte. At the end of the operation, /CS pin should be brought high. Bring /CS high after the conversion also minimizes supply current if DCLK is left running.

Table I. Control Bits in the Control Byte

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Start	A2	A1	A0	Mode1	Mode0	PD1	PD0

Table II. Descriptions of Control Bits

BIT	NAME	DESCRIPTION
7	Start	Start Bit.
6,5,4	A2,A1,A0	Input Channel Select Bits.
3,2	Mode1 Mode0	12-bit / 8-bit Conversion Configuration Bits.
1,0	PD1,PD0	Power Down Control Bits.

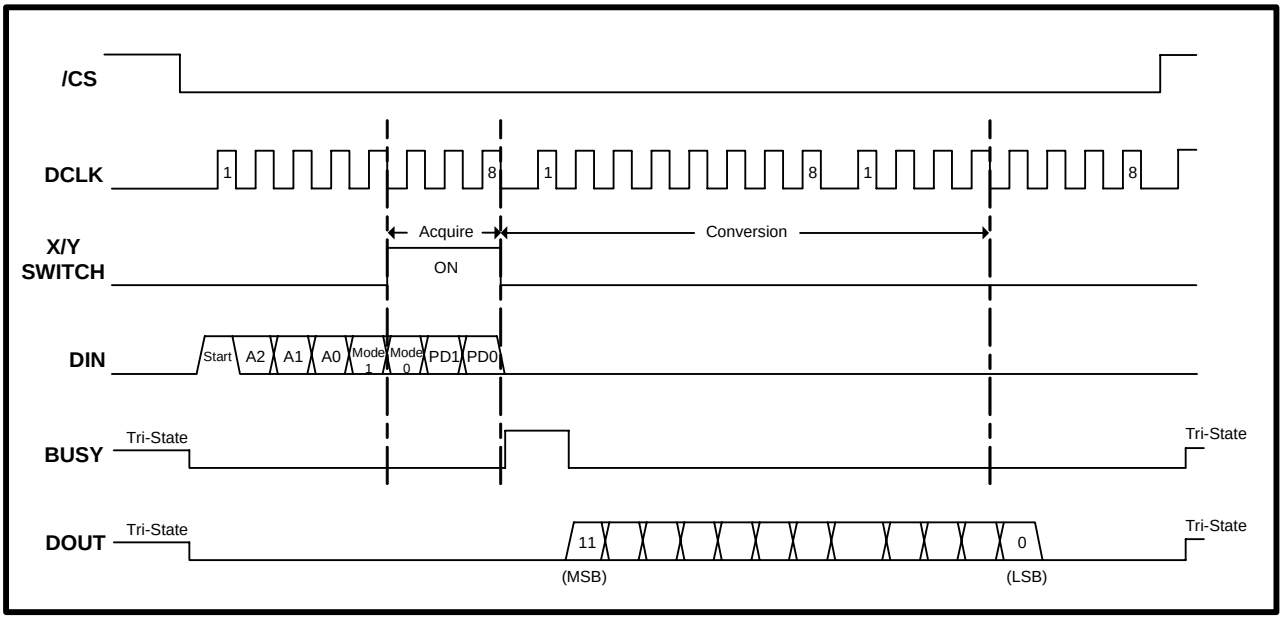


Figure 2. Serial Interface of UH7843Q/S/AQ/AS

Control Byte

Table I and Table II is detailed information of the control byte (on DIN). The control byte provides the start operation, addressing, resolution and power-down information of UH7843Q/S/AQ/AS.

Start Bit – initiate Start
The control byte starts with the first high bit on DIN. The first bit must always be high (1) to initiate the start of the conversion. UH7843Q/S/AQ/AS will ignore any inputs on DIN until the start bit is detected.

Addressing Bits – Input Channel Selection
The next three bits on the control byte (A2,A1,A0) select the active input channel of the input multiplexer (see table III and Figure 5) and the touch screen drivers (X / Y switch).

Mode Bits – Resolution and Reference Configuration
The Mode Bits (MODE1, MODE0) set the resolution and the reference input of the analog-to-digital (ADC) converter. With Mode1 bit low (0), the following conversion will have 12-bit resolution. With Mode1 bit high (1), the following conversion will have 8-bit resolution. MODE0 bit sets the reference input of the ADC (see Reference Input section and Figure 5). Table IV shows detailed information of the Mode Bits.

Power-Down Bits – Power Down Control
The last two bits (PD1, PD0) control the power-down mode and pen interrupt request of UH7843Q/S/AQ/AS. If both bits are high (1), the device is always powered up. If both bits are low (0), the device enters a power-down mode between conversions and the pen interrupt will be enabled. See Table V for more information.

Operation of 16-clocks

The typical operation of UH7843Q/S/AQ/AS is 24-clocks (three control bytes) per conversion. However, the control bits for the next conversion can be overlapped with current conversion for a faster conversion. Figure 3 shows the timing of 16-clocks conversion.

Operation of 15-clocks

The fastest operation (15 clocks per conversion) of UH7843Q/S/AQ/AS is shown in Figure 4. This operation will NOT work with the serial interface of most microcontrollers and digital signal processors, as they are not capable of providing 15 clocks cycles per serial transfer.

Table III. Input Channel Configuration

A2	A1	A0	Input Channel	X Switch	Y Switch
0	0	1	X+	OFF	ON
1	0	1	Y+	ON	OFF
0	1	0	IN3	OFF	OFF
1	1	0	IN4	OFF	OFF

Table IV. Resolution & Reference Configuration

MODE1	MODE0	Resolution	ADC Reference
0	1	12 bits	VREF
0	0	12 bits	VDD* / VREF**
1	1	8 bits	VREF
1	0	8 bits	VDD* / VREF**

* When measuring X+ (A2A1A0=001) or Y+ (A2A1A0=101)
** When measuring IN3 (A2A1A0=010) or IN4 (A2A1A0=110)

Table V. Power-Down Selection

PD1	PD0	/PENIRQ	Description
0	0	Enable	Power-down between conversions. Y-switch is on, /PENIRQ is enabled.
0	1	Disable	Power-down between conversions. Y-switch is off, /PENIRQ is disabled.
1	0	Disable	No used.
1	1	Disable	No power-down between conversions. The ADC is always powered up.

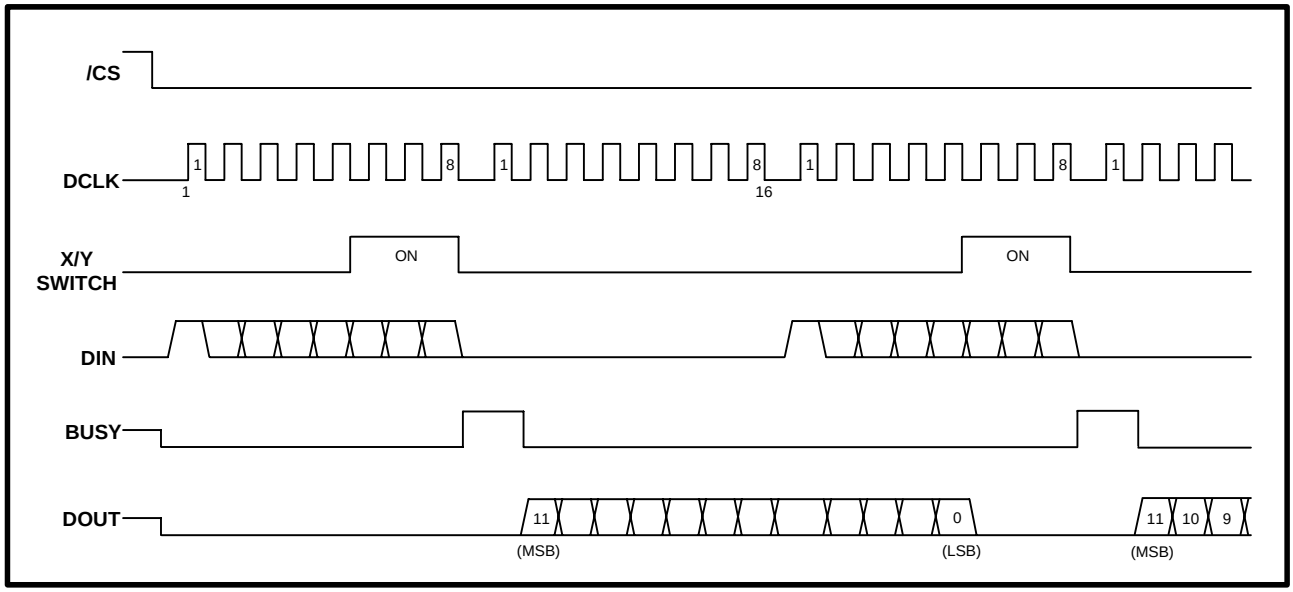


Figure 3. Timing of 16-clocks Conversions

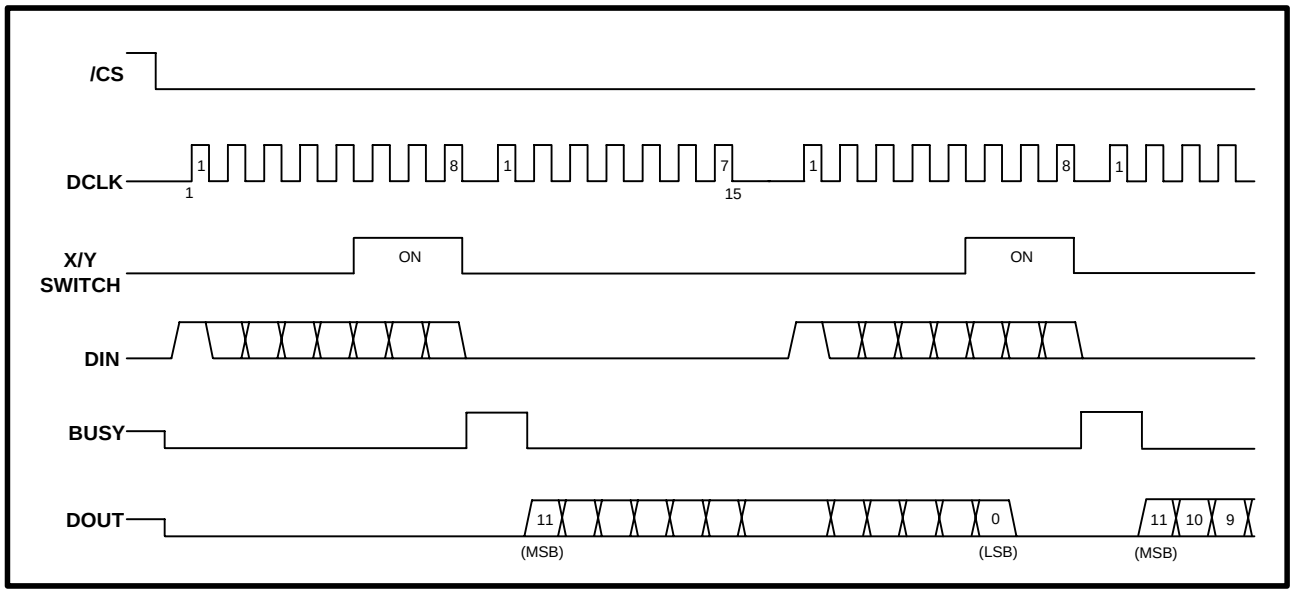


Figure 4. Timing of 15-clocks Conversions

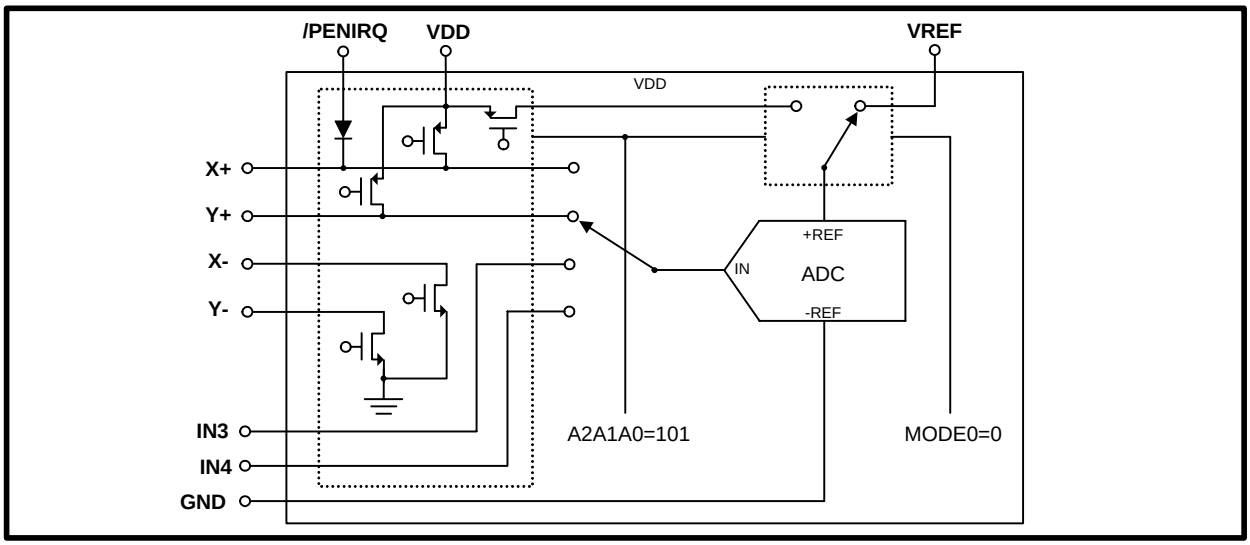


Figure 5. Diagram of Input Channel and Reference Input

ANALOG INPUT MEASUREMENT

UH7843Q/S/AQ/AS contains four channel inputs. X+ and Y+ inputs are for touch screen measurement. Two auxiliary inputs are IN3 and IN4. The input to the A/D converter is selected via the four-channel multiplexer. (See Block Diagram section and Figure 5.)

Input Channel

Table III shows the input channel configuration of UH7843Q/S/AQ/AS. The control bits are set via DIN pin. (See Control Byte section.) The selected channel is for A/D converter input. Please refer to Figure 5 for detailed input channel multiplexer. For measuring X+ and Y+, Y switches and X switches are turned on respectively.

Reference Input

UH7843Q/S/AQ/AS requires a reference input voltage source. The voltage difference between +REF and –REF (shown in Figure 5), in the range of 1V to +VDD, sets the analog-to-digital converter (ADC) input range. The full-scale analog input range of UH7843Q/S/AQ/AS is thus from 0V to VREF.

Typically the reference input is from external precise voltage source VREF (MODE0=1, see Table IV) for touch screen and auxiliary inputs measurement. Figure 6 shows the configuration for a Y coordinate measurement with MODE0=1. When utilizing the screen measurement, VREF must be equal to VDD as input range is from 0V to VDD. If the reference input is from the power supply directly, as shown in Figure 8 for example, special care must be taken to avoid noise from power supply.

When making touch screen measurements only, the reference input can be set from VDD directly (MODE0=0) and discard VREF input. Figure 7 shows the configuration for a Y coordinate measurement with MODE0=0.

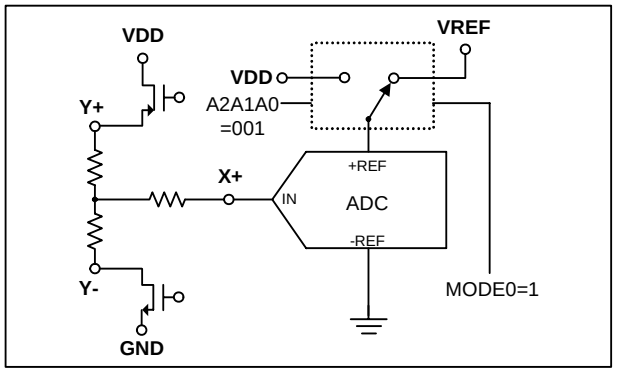


Figure 6. Touch Panel Measurement with MODE0=1

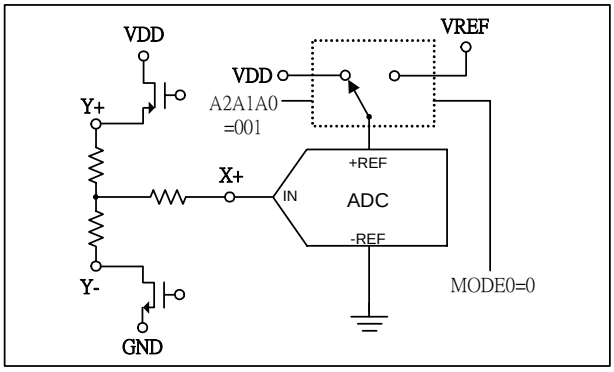


Figure 7. Touch Panel Measurement with MODE0=0

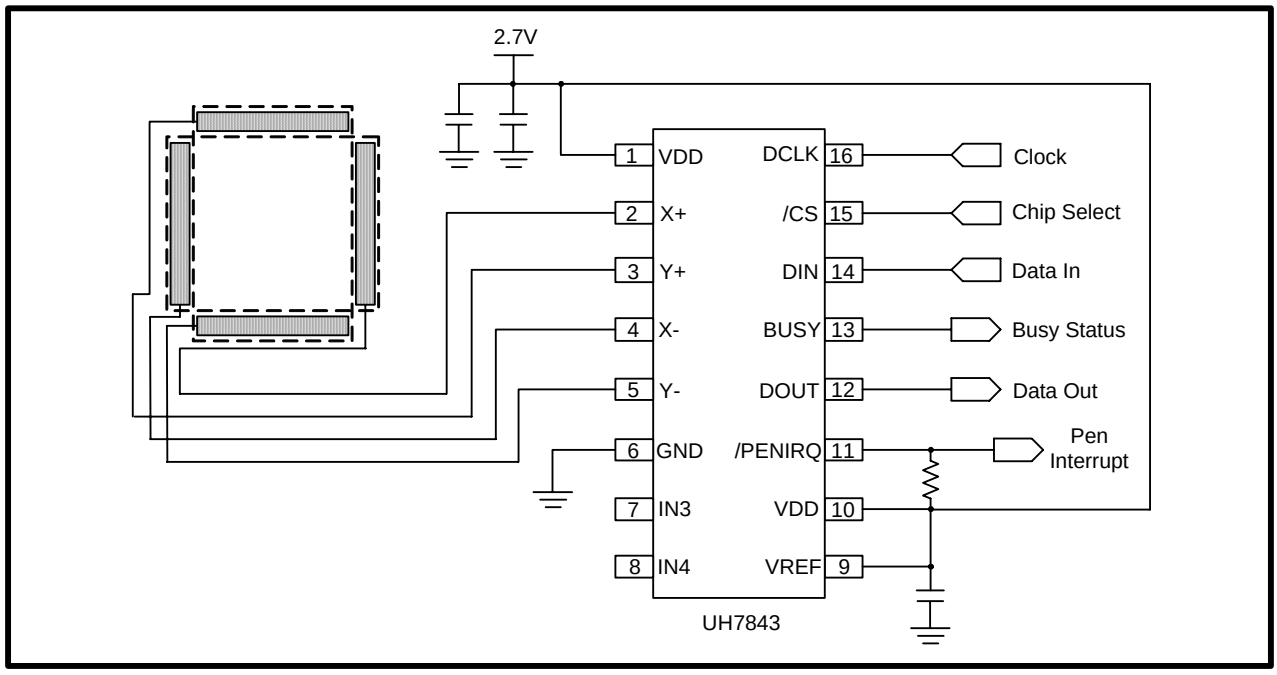


Figure 8. Typical operation of UH7843Q/S/AQ/AS

Resistive Touch Screen (4-Wire)

The 4-wire resistive touch screen consists of 2 resistive plates that are separated by a small gap. Each of the screen has a resistance in the range from 200 to 2000 ohms.

The Screen works by applying a voltage across the X plate or Y plate resistive networks. If a voltage is applied, for example, between X+ and X-, then a voltage divider is formed on the X plate. When the Y plate is touched to the X plate, a voltage will be developed on the Y plate. By accurately measuring this voltage, the touch position on the screen can be determined. The connection of UH7843Q/S/AQ/AS to the touch screen should be as short as possible.

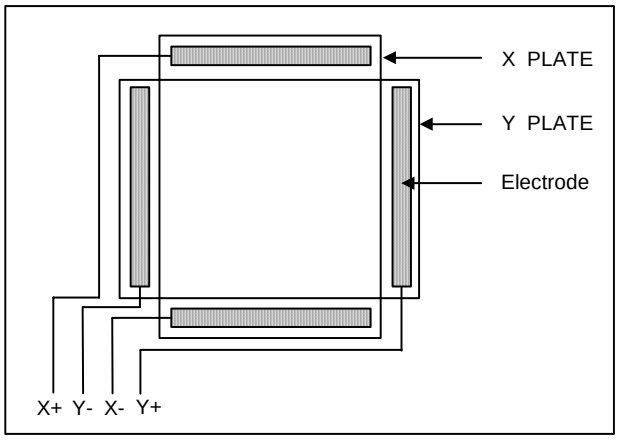


Figure 9. 4-wire Resistive Touch Panel

Pen Interrupt Request

The pen interrupt function is shown in Figure 10. Normally the /PENIRQ is HIGH by connecting a pull-up resistor (typically 100K Ω) to VDD. If /PENIRQ has been enabled (See Table V), Y- driver is ON and connected to GND and /PENIRQ diode is connected to X+ input. When the touch screen connected to UH7843Q/S/AQ/AS is touched, the X+ input in pulled to ground through the touch screen and /PENIRQ will go low to initiate an interrupt to the microprocessor.

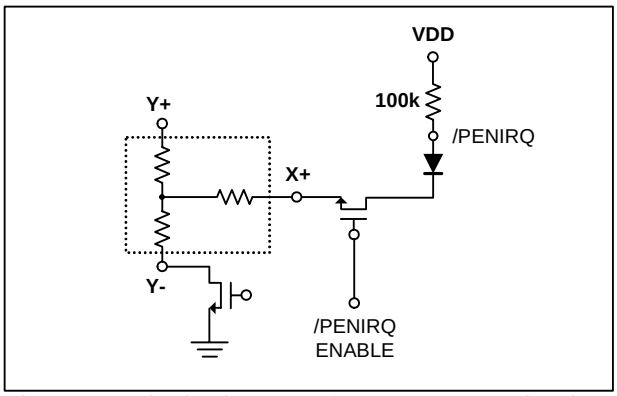
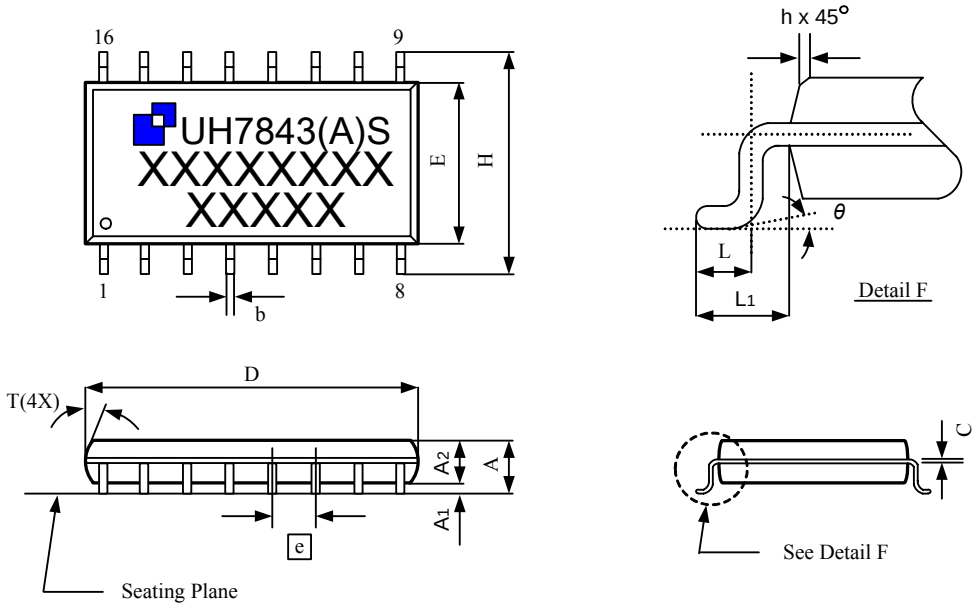


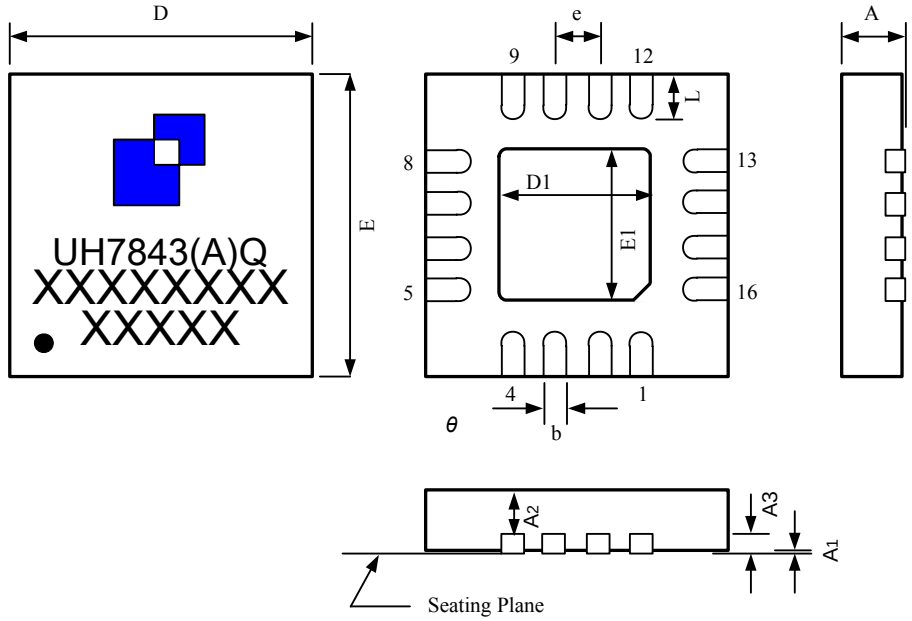
Figure 10. Block Diagram of Pen Interrupt Circuit

PACKAGE DIMENSION (SSOP-16)



SYMBOLS	DIMENSION (MM)			DIMENSION (MIL)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.60	1.75	53	63	69
A_1	0.10	0.15	0.25	4	6	10
A_2	-	-	1.50	-	-	59
b	0.20	0.254	0.30	8	10	12
C	0.18	0.203	0.25	7	8	10
D	4.80	4.90	5.00	189	193	197
E	3.80	3.90	4.00	150	154	157
H	5.80	6.00	6.20	228	236	244
e	0.635 BSC			25 BSC		
L	0.40	0.635	1.27	16	25	50
L_1	1.00	1.05	1.10	39	41	43
h	0.25	0.42	0.50	10	17	20
θ	0°	-	8°	0°	-	8°

PACKAGE DIMENSION (QFN-16)



SYMBOLS	DIMENSION (MM)			DIMENSION (MIL)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.76	0.8	0.84	30	31	33
A1	0	0.02	0.04	0	0.8	1.5
A2	0.57	0.6	0.63	22	24	25
A3	0.20 REF.			8.0 REF.		
b	0.25	0.30	0.35	9.84	11.81	13.78
D	3.90	4.00	4.10	154	157	161
D1	2.05	2.10	2.15	80.70	82.68	84.65
E	3.90	4.00	4.10	154	157	161
E1	2.05	2.10	2.15	80.70	82.68	84.65
e	0.650 BSC			25.59 BSC		
L	0.50	0.55	0.60	19.69	21.65	23.62